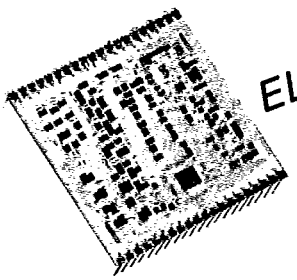
ILC DATA DEVICE CORPORATION

RDC-19190® MONOBRID® SERIES*



TACH ELIMINATOR

10, 12, 14 AND 16 BIT INDUSTRIAL RESOLVER TO DIGITAL CONVERTERS

DESCRIPTION

The RDC-19190 Series is a high performance, low cost hybrid resolver to digital converter, which also provides a high quality linear velocity output. With the introduction of the RDC-19190, bulky and expensive electromechanical tachometers may be eliminated, therefore reducing cost and increasing reliability. Control systems can now receive velocity feedback and digital conversion from one compact electronic module (2.1 x 2.1 x .27").

The "Tach Eliminator" is available to satisfy most applications. Models are available in 10, 12, 14 and 16 bit resolutions, with accuracies of ±21,±8.5, and ±2.6 respectively. Also offered are resolver or direct inputs at 11.8V and 2.0V line to line.

RDC-19190 Series is a derivative of DDC's highly successful SDC-19100 converter. Its field proven high accuracy and jitter free output is assured. Through the use of a type II tracking loop, the RDC-19190 (as with the SDC-19100) does not exhibit velocity lag up to the specified tracking rates (Figure 1).

APPLICATIONS

The RDC-19190 Series was developed specifically to facilitate savings in cost and space while increasing reliability. They may be used where both resolver to digital conversion and a linear velocity signal are required. Applications include use in motor and position control systems for robotics, CNC machine tooling and precise antenna positioning.

FEATURES:

- *TACHOMETER QUALITY VELOCITY OUTPUT ± 1.5%*
- *ABSOLUTE POSITION*
- *LOW COST*
- *WIDE OPERATING BANDWIDTH:*
  600 Hz 10 TO 14 BITS
  200 Hz 16 BITS
- *LOW POWER – 0.3 WATTS*
- *HIGH ACCURACY:*
  ± 21 MINUTES/10 BITS
  ± 8.5 MINUTES/12 BITS
  ± 2.6 ± 1LSB OR
  ± 5.3 MINUTES/14 BITS
  ± 2.6 MINUTES/16 BITS
- *INDUCTOSYN™ COMPATIBLE*

Note: Monobrid® is a registered trademark of ILC Data Device Corporation.
Inductosyn™ is a trademark of Farrand Controls Corporation.

*Patented

E

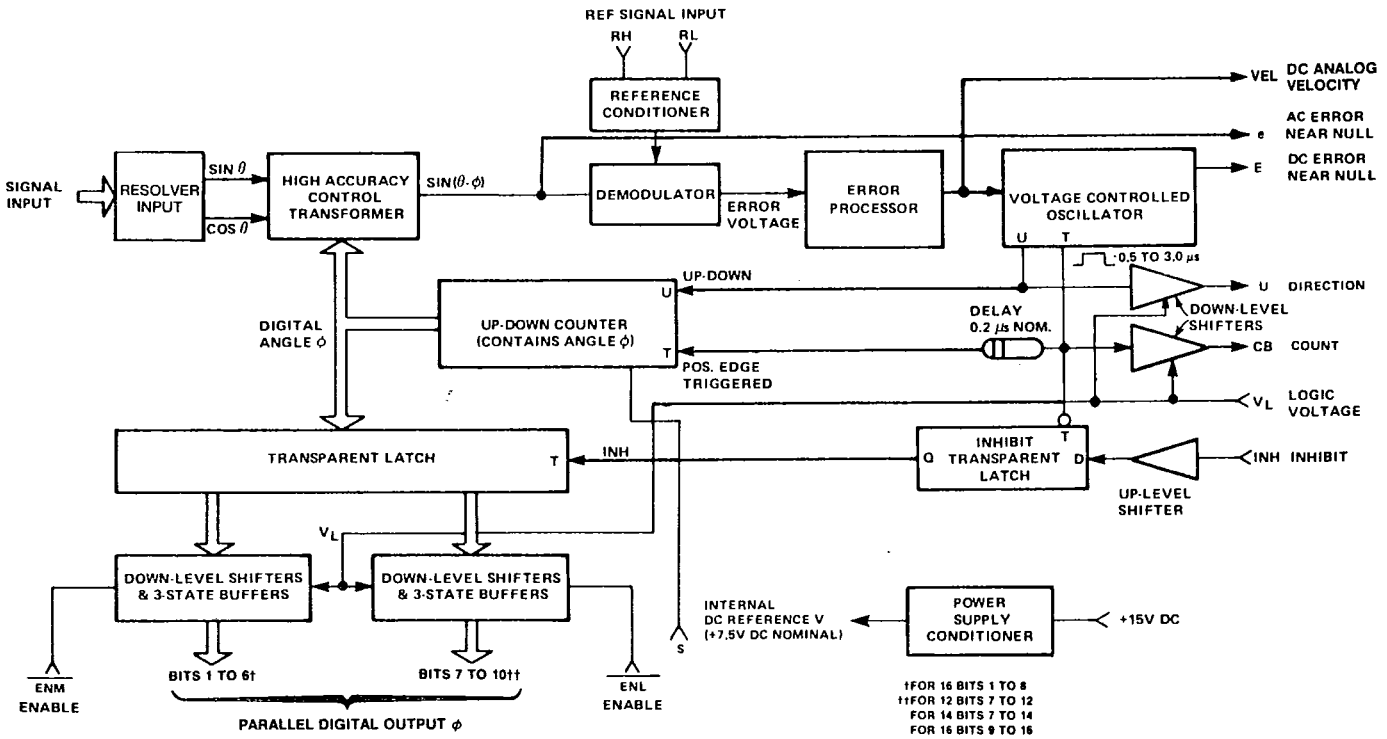


FIGURE 1. BLOCK DIAGRAM

RDC-19190 MONOBRID SERIES

ILC DATA DEVICE CORPORATION

T-71-35-03

SPECIFICATIONS
Apply over temperature range, power supply range, reference frequency and amplitude range ± 10% signal amplitude variation and up to 10% harmonic distortion in the reference.

PARAMETER	UNITS	VALUE
RESOLUTION/ACCURACY	**bits/min**	**See Model Selection Chart**
REFERENCE INPUT CHARACTERISTICS		
Voltage Range	Vrms	4 to 50
Input Impedance		
Single Ended	Ω	50k min
Differential	Ω	100 k min
Common Mode Range	V	60 max (DC common mode plus recurrent AC peak)
SIGNAL INPUT CHARACTERISTICS (Voltage options and minimum input impedance balanced)		
Resolver		11.8V L-L
Z_{in} Single Ended	Ω	27k
Z_{in} Differential	Ω	54k
Z_{in} Each (L-GND)	Ω	27k
Direct (2.0V L-L) Input Signal type		Sin and cos resolver signals referenced to converter internal DC reference V
Sin/Cos Voltage Range		2V nom, 2.3 max
Maximum Voltage Without Damage		15V rms continuous; 100V peak transient
Input Impedance		Z_{in} > 20 MΩ (transient protected voltage follower)
DIGITAL INPUT/OUTPUT		
Logic type		TTL/CMOS compatible, depending on logic supply voltage
Inputs		$Z_{in} \geq 25k\Omega$ pullup resistor to V_L
Inhibit (INH)		Logic "0" inhibit
Enable Bits 1-8 $\overline{ENM}$		
Enable Bits 1-6 $\overline{ENM}$		
Enable Bits 9-16 $\overline{ENL}$		
Enable Bits 7-14 $\overline{ENL}$		
Enable Bits 7-12 $\overline{ENL}$		
Enable Bits 7-10 $\overline{ENL}$		
$\overline{ENM}$ and $\overline{ENL}$		Logic "0" enables; Logic "1" High Impedance
S (Control Transformer) Logic Type		Logic "0" for use as CT CMOS Compatible-Logic "0" ≤ 0.3V_L, Logic "1" ≥ 0.7V_L
Loading		CMOS
Output		
Parallel Data	bits	10, 12, 14 or 16 parallel lines natural binary angle, positive logic.
Count (CB)		0.7 to 2.0 μsec positive pulse leading edge initiates counter update
Direction (U)		Logic high when counting up and logic low when counting down
Drive Capability		1 std TTL load, 1.6 mA at 0.4V max (logic "0"); 10 std TTL loads, 0.4 mA at 2.8V min (logic "1"), 10 μA max (high impedance)
ANALOG OUTPUTS		
Velocity (VEL)		
Velocity Voltage	V	See Table 1.
Scale Factor	%	10 max
Linearity	% output	1.5 max
Reversal Error	%	0.5 max
Zero Offset	mV	50 max
TC of Offset	uV/°C	25 max
Noise and Ripple		
Zero Speed	mV (rms)	15 typ
Full Speed		
10 and 12 Bits	mV (rms)	40 typ
14 and 16 bits	mV (rms)	150 typ

PARAMETER	UNITS	VALUE
Internal DC reference (V)	mV	+15 VDC/2=7.5V nom
AC Error (e)	mV	5 rms per LSB of Error (16 bits)
	mV	10 rms per LSB of Error (14 bits)
	mV	12.5 rms per LSB of Error (10 and 12 bits)
Filtered DC Error (E)	V	-0.5 per +1 LSB of error (±3 LSB range) 16 bit unit
	V	-1 per +1 LSB of error (+3 LSB range) 14 bit unit
	V	-1.25 per +1 LSB of error (±3 LSB range) 10 and 12 bit units

POWER SUPPLY CHARACTERISTICS		+15V Supply	Logic Supply
Nominal Voltage			
Voltage Range	V	+11 to +16.5	+4.5 to +15V supply
Maximum Voltage Without Damage	V	+18	+18
Current or Impedance		15 mA max	Z_{in}=5kΩ min

TEMPERATURE RANGES		
Operating		
-30X	°C	0 to +70
Storage	°C	-30 to +105

PHYSICAL CHARACTERISTICS		
Size	in	2.1 x 2.1 x 0.27 (53 x 53 x 6.9mm) See mechanical outline
Weight	oz	0.7 (20 g)

TECHNICAL INFORMATION

INTRODUCTION

The circuit shown in the RDC-19190 block diagram, Figure 1, consists of three main parts: the signal input, a feedback loop whose elements are the control transformer, demodulator error processor, VCO, and up-down counter; and digital interface circuitry including various latches and buffers.

The inputs include either resolver or direct input and produce a resolver type output for the control transformer. One input is a solid state resolver input, which accepts sine and cosine signal inputs at 11.8V L-L. The other input is a direct input of 2V L-L, which allows for use of a lower reference voltage. Since it does not have an input scaling network it is inherently more accurate.

In a resolver, shaft angle data is transmitted as the ratio of carrier amplitudes across the terminals. The internal converter operates with signals in resolver format, sin θ cos ωt and cos θ cos ωt.

Figure 2 shows resolver signals as a function of the angle θ.

The feedback loop produces a digital angle Φ which tracks the analog input angle θ to within the specified accuracy of the converter. The control transformer performs the following trigonometric computation:

$$\sin(\theta - \Phi) = \sin\theta\cos\Phi - \cos\theta\sin\Phi$$

where θ is the angle representing the resolver shaft position, and Φ is the digital angle contained in the up-down counter in the converter. The tracking process consists of continually adjusting Φ to make $(\theta - \Phi) \rightarrow 0$, so that Φ will represent the shaft position θ.

The output of the demodulator is an analog DC level proportional to sin $(\theta - \Phi)$. The error processor integrates this sin $(\theta - \Phi)$ error signal, and the output of the integrator is used to control the frequency of a voltage controlled

oscillator "clock" pulses which are accumulated by the up-down counter. The up-down counter is functionally an incremental integrator. Therefore there are two stages of integration, making the converter a type II tracking servo. In a Type II servo, the voltage controlled oscillator always settles to a counting rate which makes $d\Phi/dt$ equal to $d\theta/dt$ without lag. The output data will always be fresh and available as long as the maximum tracking rate of the converter is not exceeded.

the digital interface circuitry has three main functions: to latch the output bits during an Inhibit command so that stable data can be read out, to furnish both parallel and 3-state data formats, and to act as a buffer between the internal CMOS logic and the external logic level.

Applying an Inhibit command will lock the data in the transparent latch without interfering with the continuous tracking of the feedback loop. In the SDC-19190 Series Monobrids, therefore, the digital angle Φ is always updated and the Inhibit can be applied for an arbitrary amount of time. The Inhibit transparent latch and the 0.2 μs delay are also parts of the Inhibit circuitry, whose detailed operation is described in the Logic Output/Input Section.

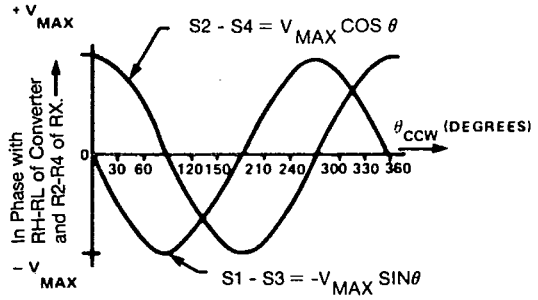
When testing or evaluating the converter, it is advisable to limit the power supply currents as follows:

+15V Supply Limit at 20 mA.
Logic Supply V_L at 2 mA + Digital Load at Logic 1.

Analog circuits inside the RDC-19190 module are referenced to an internal DC reference level V which rides at +7.5 nominal with respect to the external ground (GND). V should not be connected to the external ground.

SOLID STATE BUFFER INPUTS

The solid state signal and reference inputs are true differential inputs with high AC and DC common mode rejection. Input impedance is maintained with power off. The recurrent AC peak + DC common mode voltage should not exceed 30V peak. The maximum transient peak voltage should not exceed 150V.



Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ) With R2-R4 Excited.

FIGURE 2. RESOLVER SIGNALS

DIRECT INPUT

Direct input units require a signal conditioner that provides a 2.0V rms nominal resolver type signal referenced to the internal DC reference V.

LOGIC INPUT/OUTPUT

Logic outputs consist of parallel data bits and count (CB). All logic outputs are short-circuit proof to ground and to positive voltages as high as V_L. The CB output is a positive 0.7-2.0 μs pulse, and data changes about 0.2 μs after the leading edge of the pulse because of an internal delay (see Figure 1). Data is valid 0.5 μs after the leading edge of a CB. Angle is determined by adding bits in the 1 state.

The parallel digital outputs are gated to provide 6 and 8 bit bytes when the MSB byte is enabled ($\overline{ENM}$). The 8 bit byte is reserved for 16 bit resolution converters only. The LSB byte (ENL) is gated to provide 4, 6 and 8 bit bytes dependent upon converter resolution (4 and 6 bit bytes are reserved for 10 and 12 bit converters while the LSB byte is 8 bits for both 14 and 16 bit resolutions). When the Enables for the gates are at logic 0, the gate outputs are at normal logic 1 or 0, depending on the bit state. When the Enables are at logic 1, the gate outputs are high impedance and the bus sees an essentially open line. Outputs are valid 0.5μs after an Enable is driven to logic 0. For 10, 12, 14, or 16 bit parallel output operation when the 3-state feature is not used, the Enable lines should be tied to logic 0.

The Inhibit (INH) logic input locks the transparent latch so that the bits will remain stable while data is being transferred (see Figure 1). The output is stable 0.5 μs after the Inhibit is driven to logic 0. A logic 0 at the T input locks the latch, and a logic 1 allows the bits to change. The purpose of the INH transparent latch is to prevent the transmission of invalid data when there is an overlap between the CB and INH. While the counter is not being updated the CB is at logic 0 and the INH latch is transparent. When the CB goes to logic 1 the INH latch is locked. If a CB occurs after an INH has been applied, the latch will remain locked and its data cannot change until the CB returns to logic 0. If an INH is applied during a CB pulse, the latch will not lock until the CB pulse is over. The purpose of the 0.2 μs delay is to prevent a race condition between the CB and the INH in which the up-down counter begins to change just as an INH is applied.

The Direction Output (U) is valid as shown in Figure 3. It is logic 1 for counting up and logic 0 for counting down. Logic level at the (U) pin is valid up thru 0.5 μs before and 0.1 μs after the leading edge of the (CB) pulse.

Since RDC-19190 converters contain a CMOS device, standard CMOS handling procedures should be followed.

TIMING

Figure 3 shows the timing waveforms of the converter. Whenever an input angle change occurs, the converter changes the digital angle in 1 LSB steps and generates a converter busy pulse. The output data change is initiated

E

RDC-19190 MONOBRID SERIES

ILC DATA DEVICE CORPORATION

TABLE 1. ORDERING INFORMATION AND PERFORMANCE CHARACTERISTICS

PART NUMBER	RESOLUTION (BITS)	ACCURACY (MIN)	INPUT TYPE	SIGNAL VOLTAGE (V)	REF INPUT FREQUENCY (Hz)	TRACKING RATE (RPS)	BANDWIDTH (Hz, nom)	VELOCITY (±RPS=±V, nom)	ACCELERATION FOR 1 LSB LAG ERROR [°/SEC²]	SETTLING TIME FOR 179° STEP TO 1 LSB [ms]	Ka (X 1000)	TRANSFER FUNCTION BREAKS sec -1 exponent) A	B	A_1	A_2	
RDC-19190-301	10	±21	Resolver	11.8	2K-22K	400	815	400=3.4	1320K	10	3800	1960	750	31.9	120K	
RDC-19191-302	12	±8.5	Resolver	11.8	2K-22K	100	815	100=3.4	330K	20	3800	1960	750	31.9	120K	
RDC-19192-303	14	±5.3	Resolver	11.8	2K-22K	25	660	25=3.4	67K	30	3060	1760	750	25.7	120K	
*RDC-19192-304	14	±2.6	Resolver	11.8	2K-22K	25	660	25=3.4	67K	30	3060	1760	750	25.7	120K	
RDC-19193-304	16	±2.6	Resolver	11.8	1K-3.5K	6.3	100	6.3=3.4	1000	150	185	430	300	1.54	120K	
XDC-19194-301	10	±21	Direct	2	2K-22K	400	815	400=3.4	1320K	10	3800	1960	750	31.9	120K	
XDC-19195-302	12	±8.5	Direct	2	2K-22K	100	815	100=3.4	330K	20	3800	1960	750	31.9	120K	
XDC-19196-303	14	±5.3	Direct	2	2K-22K	25	660	25=3.4	67K	30	3060	1760	750	25.7	120K	
*XDC-19196-304	14	±2.6	Direct	2	2K-22K	25	660	25=3.4	67K	30	3060	1760	750	25.7	120K	
XDC-19197-304	16	±2.6	Direct	2	1K-3.5K	6.3	100	6.3=3.4	1000	150	185	430	300	1.54	120K	
RDC-19198-303	14	±5.3	Resolver	11.8	360-22K	12	80	14=5	1100	50	50	224	100	1.09	46K	
*RDC-19198-304	14	±2.6	Resolver	11.8	360-22K	12	80	14=5	1100	50	50	224	100	1.09	46K	
RDC-19199-304	16	±2.6	Resolver	11.8	360-3.5K	3	40	3.5=5	137	250	35	158	100	.54	46K	

*The highest accuracy grade now offered for the 14 bit resolution models is ±2.6 arc minutes +1 LSB.

The bandwidth (BW) and the acceleration constant (K_a) can be determined from the formula shown:

$BW\ (Hz) = BW\ (rad/sec)/2\pi$

$K_a = A^2$

For applications requiring zero overshoot response to a step velocity input see Figure 6. This external filter circuit is useful. Settling time is also decreased. Contact factory for additional information.

Maximum loading for each analog output is 1.0 mA. Outputs e, E, and VEL are not required for normal operation of the converter; V is used as internal DC reference with the direct input option.

The outputs e, E are not closely controlled or characterized. Consult factory for further information.

Figures 7 and 8 are 11.8V resolver and 2.0V direct input connection diagrams respectively.

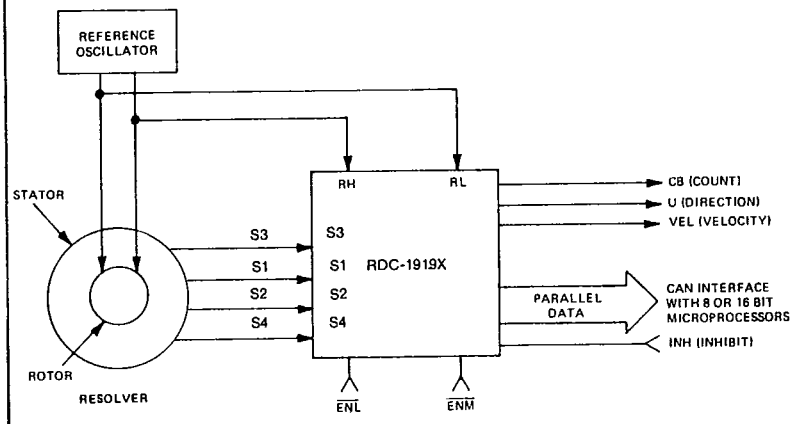


FIGURE 7. TYPICAL 11.8V RESOLVER CONNECTION

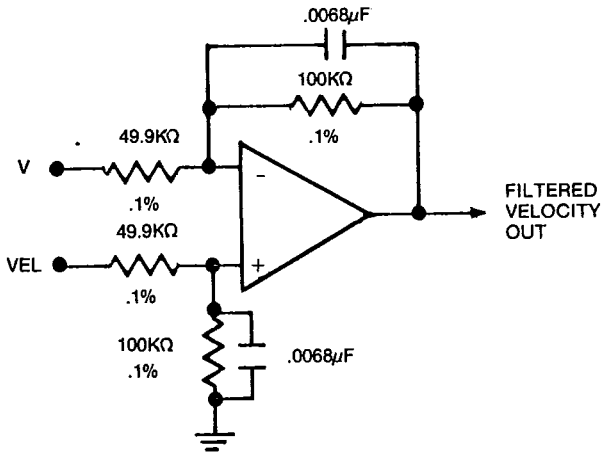


FIGURE 6. EXTERNAL FILTER CIRCUIT

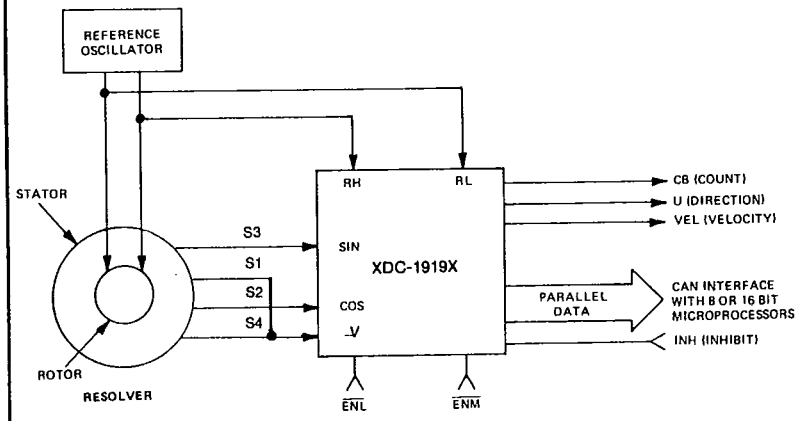


FIGURE 8. TYPICAL 2.0V DIRECT CONNECTION

by the leading edge of the CB pulse, delayed by the 0.2 μs (nominal) delay. The output becomes stable in less than 0.5 μs even though the CB pulse may last longer. Data transfer can be made synchronous with the leading edge of CB, delayed by 0.5 μs. (See Figure 3.Timing Diagram.)

An Inhibit input, regardless of its duration, does not affect converter update. A simple method of interfacing to a computer, asynchronous to CB pulse, is to (a) apply the inhibit, (b) wait 1.5 μs min., (c) transfer the data and (d) release the inhibit.

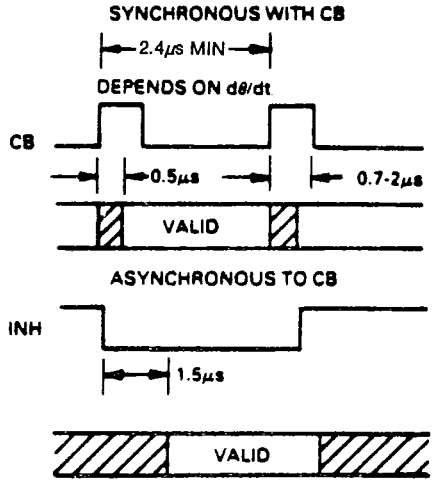


FIGURE 3. TIMING DIAGRAM

As long as the maximum tracking rate is not exceeded, there will be no lag in the converter output. If a step input occurs, as is likely when the power is initially turned on, the response will be critically damped. The figure shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot which is inherent to a Type II servo. The overshoot settling to a final value is a function of the small signal settling time.

ANALOG OUTPUTS

The analog outputs are V, e, E and VEL. V is an internal DC reference, +7.5 VDC nominal. The outputs e, E and VEL ride on the internal DC reference voltage V, and should be measured with respect to V. Outputs can swing ±5V when the voltage level of the +15V power supply is +15V. The output swing changes proportinally if the level is not a +15V.

AC error (e) is proportional to the error ($\theta - \Phi$) with 5 mV/LSB nominal for the 16 bit unit, 10 mV/LSB nominal for the 14 bit unit and 12.5 mV/LSB nominal for the 12 and 10 bit units.

E is a filtered DC voltage proportional to the error ($\theta - \Phi$) near the null point, with -0.5 VDC/+LSB of error for the 16 bit unit, -1 VDC/+LSB of error for the 14 bit unit and -1.25 VDC/+LSB of error for the 12 and 10 bit units.

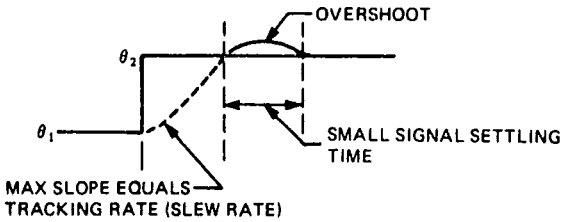
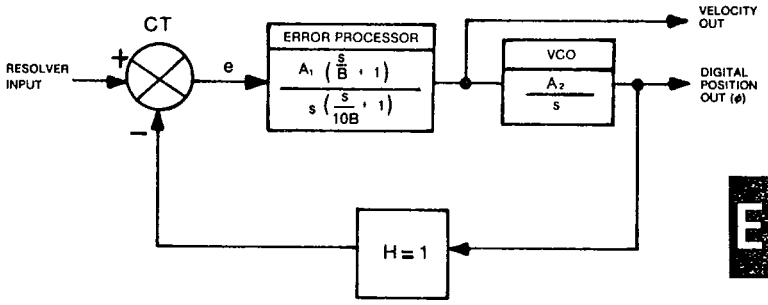


FIGURE 4. RESPONSE TO A STEP INPUT

VELOCITY

The Velocity output (VEL) from the RDC-19190 is a DC voltage proportional to angular velocity $d\theta/dt = d\phi/dt$. The velocity is the input of the second integrator as shown in Figure 5. Its linearity is dependent solely on the linearity of the voltage controlled oscillator (VCO).

Total open loop transfer function is:



$$G = \frac{A^2\left(\frac{s}{B}+1\right)}{s^2\left(\frac{s}{10B}+1\right)} \qquad \text{Where: } A^2 = A_1 A_2$$

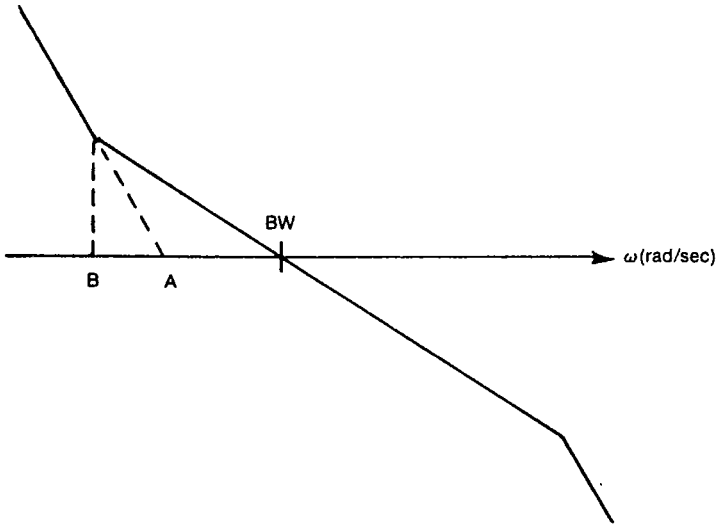


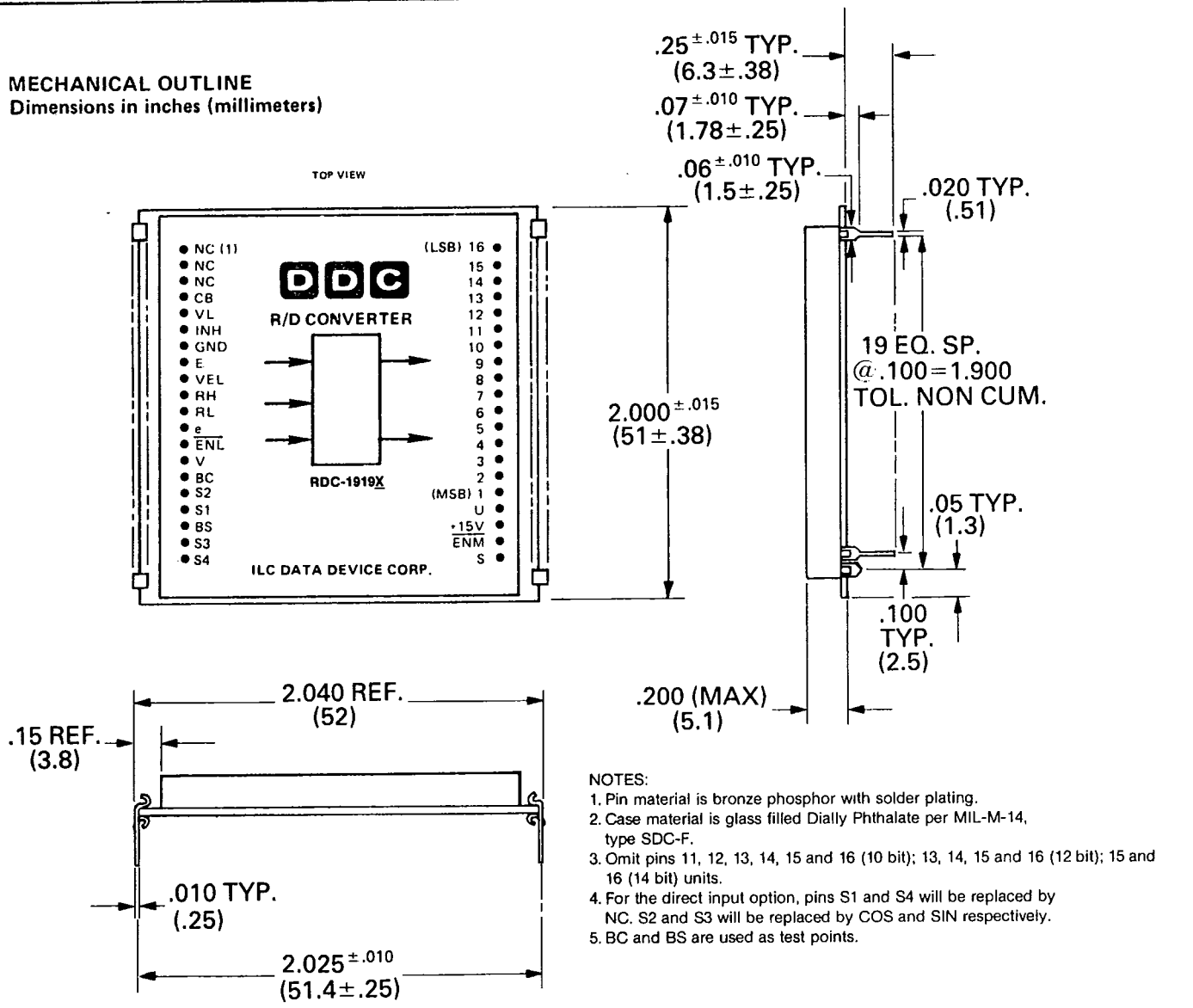
FIGURE 5. OPEN LOOP BODE PLOT

RDC-19190 MONOBRID SERIES

ILC DATA DEVICE CORPORATION

MECHANICAL OUTLINE

Dimensions in inches (millimeters)



NOTES:
1. Pin material is bronze phosphor with solder plating.
2. Case material is glass filled Dially Phthalate per MIL-M-14, type SDC-F.
3. Omit pins 11, 12, 13, 14, 15 and 16 (10 bit); 13, 14, 15 and 16 (12 bit); 15 and 16 (14 bit) units.
4. For the direct input option, pins S1 and S4 will be replaced by NC. S2 and S3 will be replaced by COS and SIN respectively.
5. BC and BS are used as test points.

ORDERING INFORMATION

See Table 1. Ordering Information and Performance Characteristics.

D-4/86